REMARKS

Claims 1-8 have been amended. Claims 9-24 have been withdrawn as to a non-elected invention. Claims 1-24 remain pending. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and foregoing remarks.

Claims 1-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,107,672 ("Hirase"). The rejection is respectfully traversed.

The present invention relates to a semiconductor device with at least three wells formed in a semiconductor substrate. At least one well is formed to have a top surface height level higher than the top surface height levels of the other two kinds of wells in relation to the top surface of the semiconductor substrate. Hirase does not disclose such a structure.

In Applicants' FIG. 2, p-well 12 is formed in a p-type substrate 10. A lightly-doped n-well 5 is formed adjacent to p-well 12. A second n-well 20, having a greater impurity concentration than the lightly-doped n-well 5 is formed on the opposite side of p-well 12. P-well 12 is formed to have a surface level (height) higher than the surface level of lightly-doped n-well 5 and n-well 20. The step level difference between wells 5, 20, and 12 is small compared to the prior art. In the prior art, FIG. 1(G), the step level difference between p-well 12 and lightly-doped n-well 5c was large, and lightly-doped n-well 5c possessed a different step level than n-well 20. Applicants' claimed structure, in contrast, does not have two different step levels (FIG. 2). Hirase does not even disclose wells having different step levels.

Hirase relates to forming a structure with p-wells 4 and 5 electrically isolated from each other (col. 2, lines, 2-18). In this manner, p-well 5 is electrically connected to substrate 1, as an NMOS region with other peripheral circuits, creating a region not having a back bias (col. 6, lines 11-14). The other p-well 4 is not electrically connected to substrate 1 and is used as a region having a back bias (col. 6, lines 5-8). Hirase is directed to the wells formation *beneath* the surface of semiconductor substrate 1. Hirase is not directed to controlling the top surface height levels of wells 4, 5, and 6a-6c.

Hirase FIGS. 1 and 4 shows p-wells 4 and 5 that are electrically isolated from each other. N-wells 6a, 6b, and 6c are formed adjacent to p-wells 4 and 5. Underneath n-well 6a is formed a deep buried well 3a. Underneath p-well 5, a deep p-well 7 is formed. Underneath n-wells 6b and 6c, a buried deep n-well 3b is formed. The buried deep n-well 3b isolates p-well 4 from substrate 1. All of Hirase's wells 4, 5, and 6a-6c, however, are formed to have the same top surface height levels (FIGS. 1 and 4).

As such, Hirase does not disclose or suggest a semiconductor device comprising, *inter alia*, "at least three kinds of wells formed in and on a top surface of [a] substrate, wherein at least one kind of well has a top surface height level higher than the top surface height levels of the other two," as recited in claim 1.

Claims 2-8 depend from claim 1 and should be allowable with claim 1 for at least the reasons provided above, and on their own merits. For example, Hirase does not disclose that the "other two kinds of wells have the same conductivity type and have different impurity concentrations with relation to each other," as recited in dependent claim 2. In Applicants' FIG. 2, lightly-doped n-well 5 has an impurity concentration smaller than n-well 20. Hirase does not disclose that n-wells 6a-6c have different impurity concentrations.

Moreover, Hirase teaches away from the subject matter of dependent claim 3. Claim 3 recites that the "other two kinds of wells have different junction depths within said substrate relative to each other." Hirase does not disclose that the wells have different junction depths; but, in fact, teaches that all of the wells have "substantially the same level in the semiconductor substrate 1." (col. 4, lines 51-52).

For example, Hirase discloses that the "buried n-well 3 and the buried p-well 7 are provided at substantially the same level in the semiconductor substrate 1." (col. 4, lines 50-52). Thus, the "bottom portions of the first p-wells 4 and 5 are at substantially the same level as the bottom portion of the n-wells 6." (col. 4, lines 52-54). Hirase does not disclose that the other two wells have different junction depths. These are additional reasons for the allowance of dependent claims 2 and 3.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

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Respectfully submitted,

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